AMENDMENTS TO THE CLAIMS

1. (Previously presented) A circuit for reducing propagation delay, comprising:

a logic circuit including a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor; and

a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage; and such that, at a voltage threshold of the logic circuit, a source-to-gate voltage of the p-type transistor is greater than a mid-supply voltage of the logic circuit, and the gate-to-source voltage of the n-type transistor is greater than the mid-supply voltage.

2. (Original) The circuit of Claim 1, wherein the logic circuit is arranged as an inverter circuit.

3. (Previously presented) A circuit for reducing propagation delay, comprising:

a logic circuit including a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor; and

a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage, wherein the voltage offset circuit includes a resistor circuit.

4. (Previously presented) The circuit of Claim 3, wherein the resistor circuit includes a plurality of resistive elements that are configured in at least one of a series or a parallel arrangement.

5. (Original) The circuit of Claim 1, wherein the voltage offset circuit includes a capacitor circuit.

6 (Previously presented) The circuit of Claim 5, wherein the capacitor circuit includes a plurality of capacitive elements that are configured in at least one of a series or a parallel arrangement.

7. (Original) The circuit of Claim 5, wherein the capacitive circuit enables an effective supply voltage that is greater than a relatively smaller supply voltage.

8. (Original) The circuit of Claim 7, wherein the effective supply voltage enables at least part of a reduction in a propagation delay associated the relatively smaller supply voltage.

9. (Original) The circuit of Claim 1, further comprising a current source circuit that is configured to provide a current.

10. (Original) The circuit of Claim 1, wherein the first voltage operates as a ramp and the second voltage operates as a relatively different ramp.

11. (Canceled)

12 (Previously presented) A timer circuit for reducing propagation delay for a relatively small supply voltage, comprising:

a current source circuit that is configured to provide a current;

a capacitor circuit that is configured to provide a first voltage in response to the current;

a voltage offset circuit that is coupled between the current source circuit and the capacitor circuit, wherein the voltage offset circuit is arranged to provide a second voltage in response to the first voltage and the current such that the second voltage is positively offset relative to the first voltage; and

an inverter circuit that includes a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor, a gate of the p-type transistor is

arranged to receive the first voltage, and a gate of the n-type transistor is arranged to receive the second voltage, wherein the voltage offset circuit includes a resistor circuit.

Claims 13-20 (Canceled)

21. (Currently amended) A circuit for reducing propagation delay, comprising:

a logic circuit including a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor, and wherein the logic circuit is coupled between a low power supply and a high power supply; and

a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage, wherein the positive offset is less than the difference between the high power supply and the low power supply; and

~~The circuit of Claim 20, further comprising~~ a current source that is operable to provide a first current, wherein the voltage offset circuit includes a resistor, and wherein the voltage offset circuit is operable to provide the first and second voltages such that the logic circuit performs as if the difference between the high power supply and the low power supply was approximately VDD+I1*R1, where I1 represents the first current, VDD represents a voltage of the high power supply high power supply, and where R1 represents the resistance of the resistor.

22. (Currently amended) ~~The circuit of Claim 20,~~ A circuit for reducing propagation delay, comprising:

a logic circuit including a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor, and wherein the logic circuit is coupled between a low power supply and a high power supply; and

a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage, wherein the positive offset is less than the difference between the high power supply and the low power supply, and wherein the

voltage offset circuit is operable to provide the first and second voltages such that the logic circuit performs as if the difference between the high power supply and the low power supply was approximately 3*VDD/2, where VDD represents a voltage of the high power supply.

23. (Previously presented) A timer circuit for reducing propagation delay for a relatively small supply voltage, comprising:

a current mirror having at least an input and an output, wherein the current mirror is arranged to receive a reference current at an input of the current mirror, and to provide a current at the output of the current mirror based on the reference current;

a capacitor circuit that is operable to provide a first voltage in response to the current;

a voltage offset circuit that is coupled between the current source circuit and the capacitor circuit, wherein the voltage offset circuit is operable to provide a second voltage in response to the first voltage and the current such that the second voltage is positively offset relative to the first voltage; and

an inverter circuit that includes a p-type transistor and an n-type transistor, wherein a drain of the p-type transistor is coupled to a drain of the n-type transistor, a gate of the p-type transistor is operable to receive the first voltage, and a gate of the n-type transistor is operable to receive the second voltage.

24. (Currently amended) A timer circuit for reducing propagation delay for a relatively small supply voltage, comprising:

a current source circuit having at least an output that is coupled to a first node, wherein the current source circuit is operable to provide a current;

a capacitor circuit that is coupled between a second node and a third node, wherein the second node is coupled to ground, and wherein the capacitor circuit is operable to provide a first voltage at the third node;

a voltage offset circuit that is coupled between the first node and the third node, wherein the voltage offset circuit is operable to provide a second voltage in response to the first voltage and the current such that the second voltage is positively offset relative to the first voltage; and

an inverter circuit that includes:

a p-type transistor having at least a gate, a drain, and a source, wherein the gate of the p-type transistor is coupled to the third node, the drain of the p-type transistor is coupled to a fourth node, and the source of the p-type transistor is coupled to a fifth node; the fifth node is a power supply node; and wherein, regardless of the logic level at the gate of the p-type transistor, the capacitor circuit is coupled between the gate of the p-type transistor and the second node; and

an n-type transistor having at least a gate, a drain, and a source, wherein the gate of the n-type transistor is coupled to the first node, the drain of the n-type transistor is coupled to the fourth node, and the source of the n-type transistor is coupled to the second node.